

Figure 1: Equivalence checking of two designs with identical state encoding

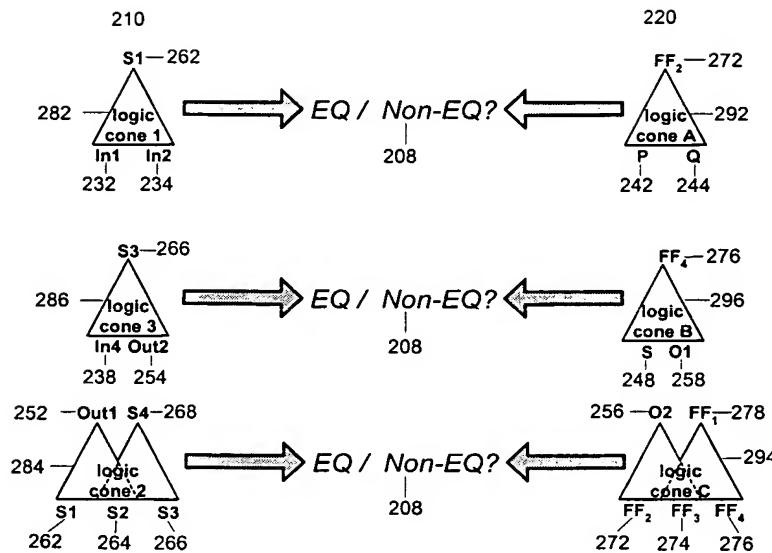


Figure 2: Comparison of logic cones of Design 1 and Design 2.

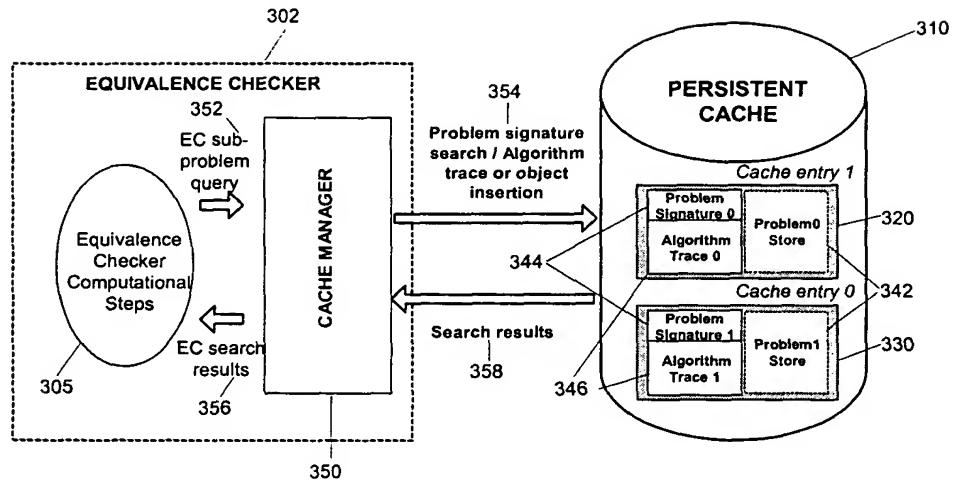


Figure 3: Persistent caches for adaptive learning

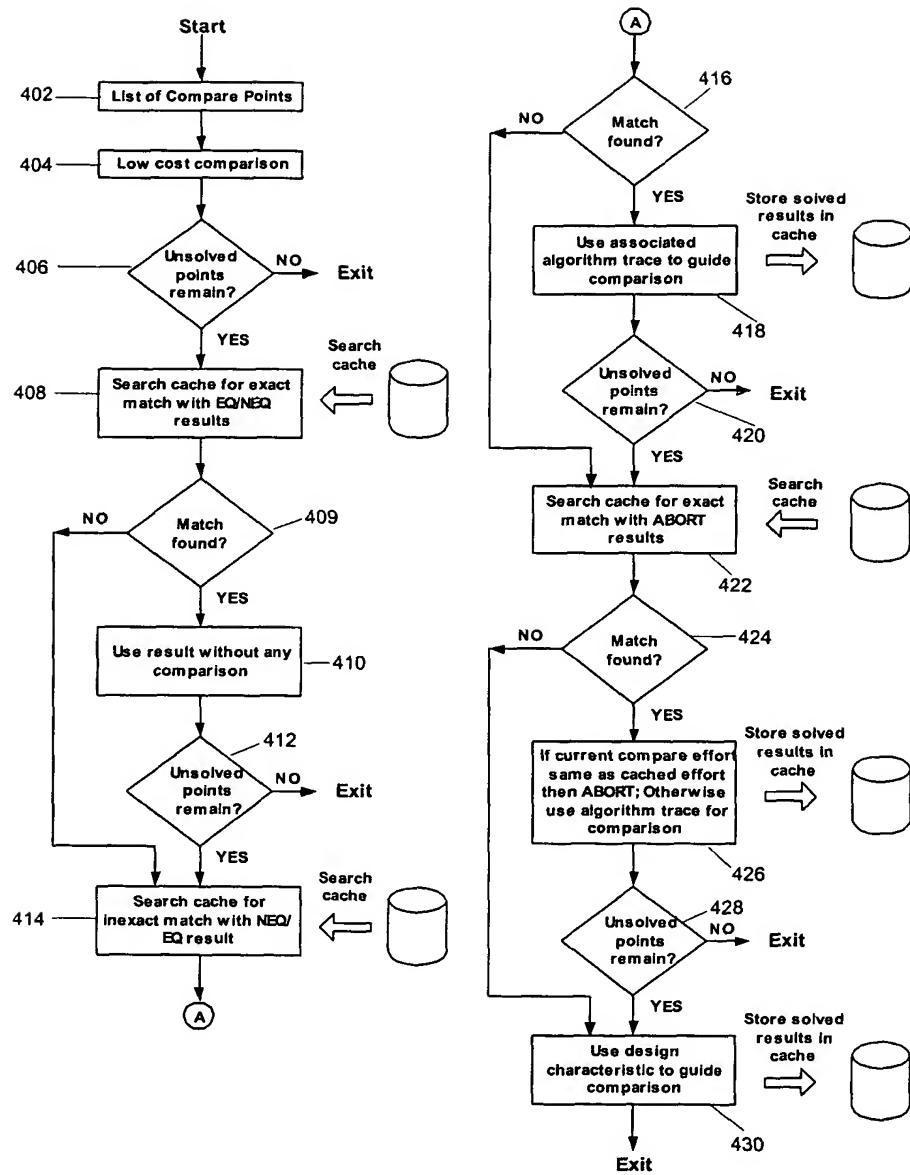


Figure 4: Compare flow with a persistent cache

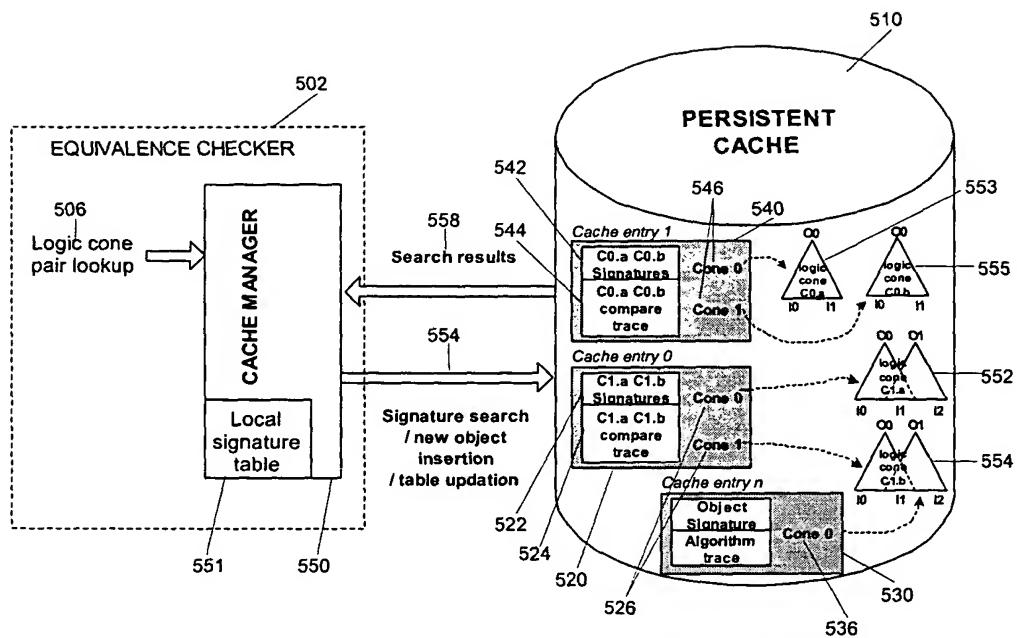


Figure 5: Logic cone pair caching in the persistent cache